What is claimed is:

1. A semiconductor memory device comprising:

a plurality of rows of memory cells;

a bank comprising a plurality of current path modifying means for substituting a redundant row of memory cells for one of the rows of memory cells;

a redundant row of memory cells;

a row address strobe circuit operable for producing a row address strobe for use in addressing rows of memory cells; and

a further current path modifying means coupled to the row address strobe circuit for controlling a speed of the row address strobe to slow the speed of the row address strobe when a redundant row of memory cells has been substituted for one of the rows of memory cells.

2. The semiconductor memory device of claim 1 wherein the further current path modifying means comprises a fuse.

3. The semiconductor memory device of claim 1 wherein the further current path modifying means comprises an antifuse.

4. The semiconductor memory device of claim 1 wherein at least one of the redundant row of memory cells is enabled and the further current path modifying means is also enabled.

5. A dynamic random access memory device comprising:

a memory array having a plurality of rows of memory cells;

a plurality of redundant rows of memory cells;

a bank of settable current path modifying means coupled to the plurality of redundant rows of memory cells for controlling a speed of a row address strobe signal to

allow sufficient additional time for using at least one of the plurality of redundant rows of memory cells;

a control circuit for providing a row address strobe signal for accessing the memory cells; and

a further settable current path modifying means additional to and adjacent to the bank of current path modifying means coupled to the control circuits.

6. The dynamic random access memory device of claim 5, wherein setting the further settable current path modifying means sets the control circuit to introduce a delay in providing of the row address strobe signal.

7. The dynamic random access memory device of claim 5 wherein the further settable current path modifying means comprises a fuse.

8. The dynamic random memory device of claim 5 wherein the further settable current path modifying means comprises an antifuse.

9. The dynamic random memory device of claim 5 wherein at least one of the redundant rows of memory cells is enabled and the further settable current path modifying means is also enabled.

10. A computer system, the computer system comprising a memory device, the memory device including:

a plurality of rows of memory cells;

a redundant row of memory cells;

a bank of current path modifying means settable for substituting one or more redundant rows of memory cells for one or more of the plurality of memory cells;

a row address strobe circuit operable for producing a row address strobe; and

a further current path modifying means coupled to the row address strobe circuit and settable independently of the bank of current path modifying means for controlling a speed of the row address strobe.

11. The computer system of claim 10, wherein the memory device is a dynamic random access memory (DRAM).

12. The computer system of claim 10 wherein the memory device is selected from the group consisting essentially of SDRAM, DDR SDRAM, SLDRAM, Direct RDRAM, SRAM, VRAM, EEPROM, and Flash memories.

13. The computer system of claim 10 wherein the further current path modifying means comprises a fuse.

14. The computer system of claim 10 wherein the further current path modifying means comprises an antifuse.

15. A semiconductor memory, comprising:

a plurality of rows of memory cells;

a plurality of rows of redundant memory cells each of the plurality of rows of redundant memory cells coupled to one of a plurality of current path modifying means for enabling the row of redundant memory cells, each of the plurality of rows of redundant memory cells capable of replacing one of the plurality of rows of memory cells upon changing the state of its current path modifying means;

a row address strobe circuit operable for producing a row address strobe signal; and

further current path modifying means coupled to a control input of the row address strobe circuit to control a speed of the row address strobe signal independently of the plurality of current path modifying means.

16. The semiconductor memory of claim 15 wherein the further current path modifying means comprises a fuse.

17. The semiconductor memory of claim 15 wherein the further current path modifying means comprises an antifuse.

18. A dynamic random access memory device, comprising:

a plurality of rows of memory cells;

a plurality of rows of redundant memory cells, each of the plurality of redundant memory cells having a first current path modifying means for replacing one of the plurality of rows of memory cells upon changing a state of the first current path modifying means;

a row address strobe circuit operable for producing a row address strobe signal; and

a second current path modifying means for conmtrolling a speed of the row address strobe signal, said means coupled to a control input of the row address strobe circuit and settable independently of the first current path modifying means.

19. The dynamic random access memory device of claim 18 wherein the further current path modifying means comprises a fuse.

20. The dynamic random access memory device of claim 18 wherein the further current path modifying means comprises an antifuse.

21. A method for slowing a row address strobe signal of a memory device, comprising:

enabling a row of redundant memory cells by setting a first current path modifying means in the row of redundant memory cells; and

setting a second current path modifying means to delay the row address strobe signal.

22. The method of claim 18 wherein the second current path modifying means comprises a fuse.

23. The method of claim 18 wherein the second current path modifying means comprises an antifuse.

24. A method of delaying a row address strobe signal in a memory device, comprising:

setting a first current path modifying means of a redundant row of memory cells;

setting a second current path modifying means in response to setting of the first current path modifying means; and

delaying the row address strobe signal in response to setting the second current path modifying means.

25. The method of claim 24 wherein the second current path modifying means comprises a fuse.

26. The method of claim 24 wherein the second current path modifying means comprises an antifuse.

27. A method for controlling row address strobe signal speed in a row address strobe chain of a memory device, comprising:

coupling a first current path modifying means to delay circuitry having a known delay; and

setting a second current path modifying means to couple the delay circuitry to the row address strobe chain to delay the row address strobe signal if a row of redundant memory cells is enabled in the memory device.

28. The method of claim 27, wherein coupling the delay circuitry comprises setting the first current path modifying means.

29. The method of claim 27 wherein the second current path modifying means comprises a fuse.

30. The method of claim 27 wherein the second current path modifying means comprises an antifuse

31. A method of delaying row address strobe signals in a semiconductor memory device, comprising the steps of:

enabling a spare row of memory cells by setting a first current path modifying means; and

setting a second current path modifying means in a state to delay the row address strobe signals when a spare row of memory cells is enabled.

32. The method of claim 31 wherein the second current path modifying means comprises a fuse.

33. The method of claim 31 wherein the second current path modifying means comprises an antifuse.

34. A memory device, comprising:

an address circuit for receiving memory address and accessing a plurality of primary memory rows or a plurality of redundant memory rows;

a bank of first current path modifying means coupled to the address circuit for selective programming access to at least one of the plurality of redundant memory rows;

second current path modifying means directly connected to a control input of the row address strobe circuit to for switching the row address strobe circuit between the first, fast mode and the second, slow mode; and

a row address strobe circuit operable in a first, fast mode and a second, slower mode, the second, slower mode selectable by separately operating the second current path modifying means.

35. The memory device of claim 34 wherein the further current path modifying means comprises a fuse.

36. The memory device of claim 34 wherein the further current path modifying means comprises an antifuse.

37 The memory device of claim 34 wherein at least one of the redundant row of memory cells is enabled and the further current path modifying means is also enabled.

38. A semiconductor memory device comprising:

a plurality of rows of memory cells;

a fuse bank comprising a plurality of fuses, each connected for substituting a redundant row of memory cells for one of the rows of memory cells;

a redundant row of memory cells;

a row address strobe circuit operable for producing a row address strobe for use in addressing rows of memory cells; and

an antifuse fuse coupled to the row address strobe circuit, the antifuse settable to control a speed of the row address strobe to slow the speed of the row address strobe when a redundant row of memory cells has been substituted for one of the rows of memory cells.

39. The semiconductor memory device of claim 38 wherein the antifuse comprises a laserfuse.

40. The semiconductor memory device of claim 38 wherein the at least one of the plurality of fuses of the fuse bank comprises an antifuse.

41. The semiconductor memory device of claim 38 wherein at least one of the redundant row of memory cells is enabled and the antifuse is also enabled.

42. A dynamic random access memory device comprising:

a memory array having a plurality of rows of memory cells;

a plurality of redundant rows of memory cells;

a bank of fuses coupled to the plurality of redundant rows of memory cells;

a control circuit for providing a row address strobe signal for accessing the memory cells; and

an antifuse coupled to the control circuit to control a speed of the row address strobe signal when the antifuse is set.

43. The dynamic random access memory device of claim 42, wherein setting the antifuse sets the control circuit to introduce a delay in providing of the row address strobe signal.

44. The dynamic random access memory device of claim 42 wherein setting the antifuse controls the speed of the row address control signal to allow sufficient time for using at least one of the plurality of redundant rows of memory cells.

45. A computer system, the computer system comprising a memory device, the memory device including:

a plurality of rows of memory cells;

a redundant row of memory cells;

a fuse bank for substituting one or more redundant rows of memory cells for one or more of the plurality of memory cells;

a row address strobe circuit operable for producing a row address strobe; and

an antifuse coupled to the row address strobe circuit and settable independently of the fuses for controlling a speed of the row address strobe.

46. The computer system of claim 45, wherein the memory device is a dynamic random access memory (DRAM).

47. The computer system of claim 45 wherein the memory device is selected from the group consisting essentially of SDRAM, DDR SDRAM, SLDRAM, Direct RDRAM, SRAM, VRAM, EEPROM, and Flash memories.

48. A semiconductor memory, comprising:

a plurality of rows of memory cells;

a plurality of rows of redundant memory cells each of the plurality of rows of redundant memory cells coupled to one of a plurality of fuses to enable the row of redundant memory cells, each of the plurality of rows of redundant memory cells to replace one of the plurality of rows of memory cells upon changing the state of its fuse;

a row address strobe circuit to produce a row address strobe signal; and

at least one antifuse coupled to a control input of the row address strobe circuit, the at least one antifuse settable to control a speed of the row address strobe signal.

49. The semiconductor memory of claim 48 wherein the control of the speed of the row address strobe signal is independent of the state of the fuses,

50. The semiconductor memory of claim 48 wherein at least one of the plurality of rows of redundant memory cells is enabled and the antifuse is set.

51. A dynamic random access memory device, comprising:

a plurality of rows of memory cells;

a plurality of rows of redundant memory cells each of the plurality of rows of redundant memory cells having a first fuse, each of the plurality of rows of redundant memory cells capable of replacing one of the plurality of rows of memory cells upon changing the state of its first fuse;

a row address strobe circuit operable for producing a row address strobe signal; and

an antifuse coupled to a control input of the row address strobe circuit, the antifuse settable independently of the first fuses.

52. The dynamic random access memory device of claim 51 wherein setting the antifuse controls a speed of the row address strobe signal.

53. A method for slowing a row address strobe signal of a memory device, comprising:

enabling a row of redundant memory cells by setting a fuse in the row of redundant memory cells; and

setting an antifuse to delay the row address strobe signal.

54. A method of delaying a row address strobe signal in a memory device, comprising:

setting a fuse of a redundant row of memory cells;

setting an antifuse in response to setting of the fuse; and

delaying the row address strobe signal in response to setting the antifuse.

55. A method for controlling row address strobe signal speed in a row address strobe chain of a memory device, comprising:

coupling an antifuse to delay circuitry having a known delay; and

setting the antifuse to couple the delay circuitry to the row address strobe chain to delay the row address strobe signal if a row of redundant memory cells is enabled in the memory device.

56. The method of claim 55, wherein coupling the delay circuitry comprises setting the antifuse.

57. A method of delaying row address strobe signals in a semiconductor memory device, comprising the steps of:

enabling a spare row of memory cells by setting a first fuse; and

setting an antifuse to a state to delay the row address strobe signals when a spare row of memory cells is enabled.

58. A memory device, comprising:

an address circuit for receiving memory address and accessing a plurality of primary memory rows or a plurality of redundant memory rows;

a fuse bank coupled to the address circuit for selective programming access to at least one of the plurality of redundant memory rows;

an antifuse directly connected to a control input of the row address strobe circuit to for switching the row address strobe circuit between the first, fast mode and the second, slow mode; and

a row address strobe circuit operable in a first, fast mode and a second, slower mode, the second, slower mode selectable by separately operating the antifuse when the fuse bank selectively programs access to at least one of the plurality of redundant memory rows.

59. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

enabling a spare row of memory cells by setting a fuse in a fuse bank; and

setting an antifuse to delay the row address strobe signals.

60. The method of claim 59, wherein the row address strobe signals are delayed more than approximately 2 nanoseconds.

61. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

enabling a spare row of memory cells; and

setting a slow down antifuse, separate from enabling a spare row of memory cells, in a state to delay the row address strobe signals, wherein setting the antifuse occurs substantially simultaneously with enabling the spare row of memory cells.

62. The method of claim 61, wherein the spare row of memory cells are enabled by setting a fuse.

63. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

probe testing the memory device at a wafer level;

detecting a bad row of memory cells;

setting a redundancy fuse to enable a spare row of memory cells for use in place of the bad row of memory cells; and

setting a fast/slow antifuse in a state to delay the row address strobe signals independent of enabling the spare row of memory cells in conjunction with enabling the spare row of memory cells for use in place of the bad row of memory cells.

64. The method of claim 63 wherein the redundancy fuse and the fast/slow antifuse are set at approximately the same time.

65. The method of claim 63 wherein multiple redundancy fuses are set.

66. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

providing redundant rows of memory cells; and

coupling a fast/slow antifuse by a conductive line to a control logic in the semiconductor memory device, the fast/slow antifuse set in a condition to slow down a row address strobe chain, wherein the fast/slow antiuse is set to another condition when no redundant rows are enabled.

67. The method of claim 66, wherein the method further includes delaying the row address strobe signals by more than approximately 2 nanoseconds.

68. The method of claim 66, wherein coupling a fast/slow antifuse includes coupling a laser fuse.

69. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

testing the semiconductor memory device at a wafer level;

determining if the semiconductor memory device has a defective row of memory cells;

remapping a unique row address associated with the defective row of memory cells to a spare row of memory cells; and

setting a fast/slow antifuse to delay the row address strobe signals in conjunction with remapping the unique row address, wherein setting the fast/slow antifuse is independent of remapping the unique row address.

70. The method of claim 69, wherein setting the fast/slow antifuse occurs before remapping the unique row address.

71. The method of claim 69, wherein setting the fast/slow antifuse occurs after remapping the unique row address.

72. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

testing the semiconductor memory device at a wafer level;

determining if the semiconductor memory device has a defective row of memory cells;

remapping a unique row address associated with the defective row of memory cells to a spare row of memory cells; and

setting a fast/slow antifuse to delay the row address strobe signals substantially simultaneously with remapping the unique row address, wherein setting the fast/slow antifuse is independent of remapping the unique row address.

73. The method of claim 72, wherein the method further includes delaying the row address strobe signals by more than approximately 2 nanoseconds.

74. A method of delaying row address strobe signals in a semiconductor memory device, comprising:

remapping a unique row address associated with a defective row of memory cells to a spare row of memory cells; and

setting an antifuse to delay the row address strobe signals in conjunction with remapping the unique row address, wherein setting the antifuse is independent of remapping the unique row address.

75. The method of claim 74, wherein setting the antifuse occurs substantially simultaneously with remapping the unique row address.

76. The method of claim 74, wherein setting the antifuse occurs before remapping the unique row address.